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Hall Ticket Number:

Code No.: 6132 M

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.E. (CBCS : ECE) I-Semester Make up Examinations, March-2017

(Embedded Systems & VLSI Design)

Digital IC Design

Time: 3 hours Max. Marks: 70

*Note: i. Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

ii. Use 250/100 nm technology parameters wherever necessary. Mention clearly assumptions made, if any.

Part-A (10 × 2 = 20 Marks)

1. List two serious VLSI design challenges in DSM regime and suggest how to manage them.
2. List four important design metrics for evaluating VLSI circuit performance and comment on their trade-offs.
3. Implement EXOR / EXNOR function using Complementary Pass-transistor Logic.
4. How do you compensate for the charge leakage in a dynamic logic NAND2 circuit?
5. Distinguish a dynamic CMOS latch from a static CMOS latch, giving neat circuits.
6. Give two sources of power-grid noise in a VLSI chip. How do you mitigate them?
7. Justify how dual V_{th} transistors reduce power consumption in a VLSI system.
8. Compare a carry bypass adder with a ripple carry adder in terms of speed and area.
9. Draw a 3T DRAM cell. Draw its Read and Write timing diagrams.
10. What is the need for a sense amplifier in RAM structures? Give its topology.

Part-B (5 × 10 = 50 Marks)

11. a) List the VLSI design abstraction levels and justify the need for them with an example. [4]

    b) Estimate the propagation delay, t_{pd} and Noise Margins, NM_L and NM_H for a skewed CMOS inverter sized as $(W/L)_P / (W/L)_N = (5/1)$. [6]

12. a) Compare a Transmission Gate (TG) logic with an NMOS/PMOS pass transistor logic. Plot the R_{eq} vs V_{out} for a TG and interpret. [4]

    b) Implement the logic function F = AB + CD in CMOS using AOI gates. Calculate the minimum delay for computing F and size the transistors to achieve this. Assume each input can present a load of 20 λ of transistor width and an output load of 100 λ of transistor width. [6]

13. a) Draw the schematic of an NMOS only pass transistor based Master-slave register. How does clock-overlap affect its performance? Generate a non-overlapping clock which will avoid this problem. [4]

    b) A function log (|a + b|) is to be implemented using three modules, namely, adder, absolute value and log computers. Given t_{pd} of each of these modules is 10ns (approx) and the registers used have a set up time of 20 ps and $t_{c\text{-}q}$ delay of 100 ps, compute the maximum clock frequency at which this system works correctly. By how much can you improve the performance by pipelining? What is the latency? [6]

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14. a) Briefly explain the principle of operation of a Carry-Lookahead Adder (CLA) with the help of a conceptual diagram. How is the ripple effect eliminated? What are its limitations? [6]

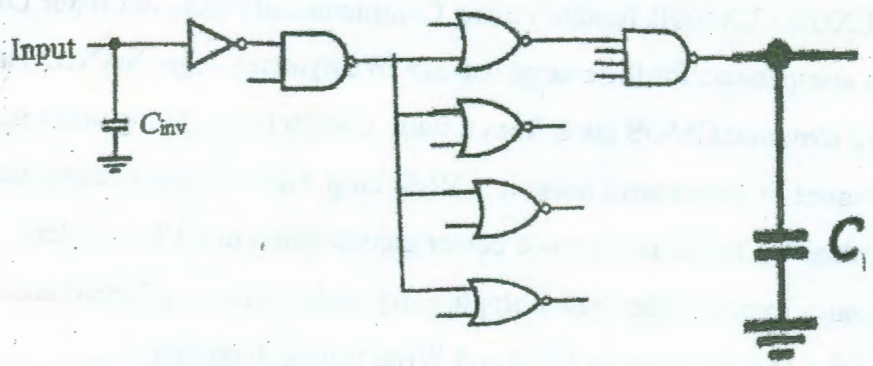
b) A CMOS VLSI chip in 1.2 V, 100 nm process has 200 million transistors, of which 20 million are in logic gates and rest in memory arrays. Logic and memory transistors are 12λ and 4λ wide with activities 0.1 and 0.05 respectively. Assuming the transistors have a gate capacitance of 2fF/μm, estimate the dynamic power consumption per MHz of the system. [4]

15. a) Compare and contrast a resistive load SRAM cell with a standard 6T SRAM cell with suitable schematics. [4]

b) Draw the architecture of a 128 K SRAM organized as a 512 × 256 core array. Estimate the word-line and bit-line capacitances assuming $C_g = 2fF$, $C_{sd} = 0.5$ fF and $C_w = 0.2$ fF. [6]

16. a) Give the Elmore delay model for a CMOS NAND 8 and estimate its propagation delay assuming a 0.1 pF load. [4]

b) Consider a data path shown below. Select gate sizes to minimize delay in the data path. [6]



17. Write short notes on any *two* of the following:

a) Memory Reliability [5]

b) 4 bit Barrel Shifter [5]

c) TSPC register. [5]